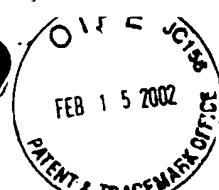


Docket No.: L&L-I0178



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Lothar Risch et al.  
Applic. No. : 09/996,279  
Filed : November 28, 2001  
Title : Double Gate MOSFET Transistor and Method for the Production Thereof

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ORIGINALLY FILED

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INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,  
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,120,666 (Gotou), dated June 9, 1992;

United States Patent No. 5,646,058 (Taur et al.), dated July 8, 1997;

German Patent DE 44 33 086 C2 (Maegawa), dated March 30, 1995, semiconductor device and method for producing it;

German Published, Non-Prosecuted Patent Application DE 198 03 479 A1 (Miyamoto et al.), dated December 24, 1998, semiconductor device and production method for a semiconductor device;

European Patent Application EP 0 612 103 A2 (Rhee), dated August 24, 1994.

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European Patent Application EP 0 704 909 A2 (Cunningham et al.), dated April 3, 1996;

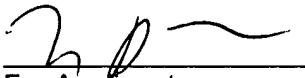
Colinge, J.P. et al.: "Silicon-On-Insulator 'Gate-All-Around Device'", IEDM 1990, pp. 595-598;

Wong, Hon-Sum Philip et al.: "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel", IEDM 1997, pp. 427-430;

Pikus, F.G. et al.: "Nanoscale field-effect transistors: An ultimate size analysis", Appl. Phys. Lett. 1971, Vol. 25, December 22, 1997, pp. 3661-3663.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

  
For Applicants

Date: January 7, 2002

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